Amdahl 470

MANAGEMENT SUMMARY

In a world dominated by one company, Amdahl's 470 systems have carved out a highly successful track record against such formidable opposition as the IBM 303X Series. Since the company's founding in 1971, Amdahl's policy has been to introduce technically advanced, innovative, large-scale systems that match or exceed IBM step for step.

The 470 product line includes four models in the 470V/7 Series: the 470V/7C, 470V/7B, 470V/7A, and 470V/7, and the top-of-the-line 470V/8. The newest model, the 470V/7C, was announced in November, 1980, about a week after IBM announced its 3033S processor. In typical PCM fashion, the 470V/7C is about 8 percent more powerful than the 3033S, and costs about 12 percent less. Amdahl's 470V/7B and 470V/7A bracket IBM's 3033N in performance. The 470V/7B has about 8 percent less and the 470V/7A has about 10 percent more power than the 3033N. The 470V/7 has about 10 percent more power than the 3033U, and the 470V/8 has about 25 to 30 percent more power than the 3033U, according to Amdahl. The 470V/7C is field-upgradeable to the 470V/8.

While Amdahl's 470 product line does not include attached-processor or multiprocessor configurations, its 470V/8 price/performance is highly competitive with IBM's biggest. For example, a 470V/8 with 16 megabytes of memory and 24 channels costs $3,200,000. A 3033AP (using the 3042 Model 2 Attached Processor) with the same memory size and 18 channels costs $4,518,500. A 3033MP with 16 megabytes of memory and 24 channels costs $5,436,000. In performance the Amdahl 470V/8 is estimated at about 6.4 MIPS (million instructions per second), and its IBM counterparts both clock in with about 8.5 MIPS. Amdahl's price per MIP, however, is ➢

Since the installation of its first 470V/6 in 1975, to the November 1980 announcement of the new 470V/7C and 580 Series, Amdahl Corporation has set the pace for the plug-compatible mainframe industry. The five current models in the 470 family offer up to 16 megabytes of main memory, up to 32 channels, and compete head-to-head with IBM's 303X Series.

CHARACTERISTICS

MANUFACTURER: Amdahl Corporation, 1250 East Arques Avenue, Sunnyvale, California 94086. Telephone (408) 746-6000.

CURRENT MODELS: Amdahl 470V/7C, 470V/7B, 470V/7A, 470V/7, and 470V/8.

PRIOR MODELS: Amdahl 470V/5, 470V/5-II, 470V/6, and 470V/6-II.

DATE ANNOUNCED: See characteristics chart.

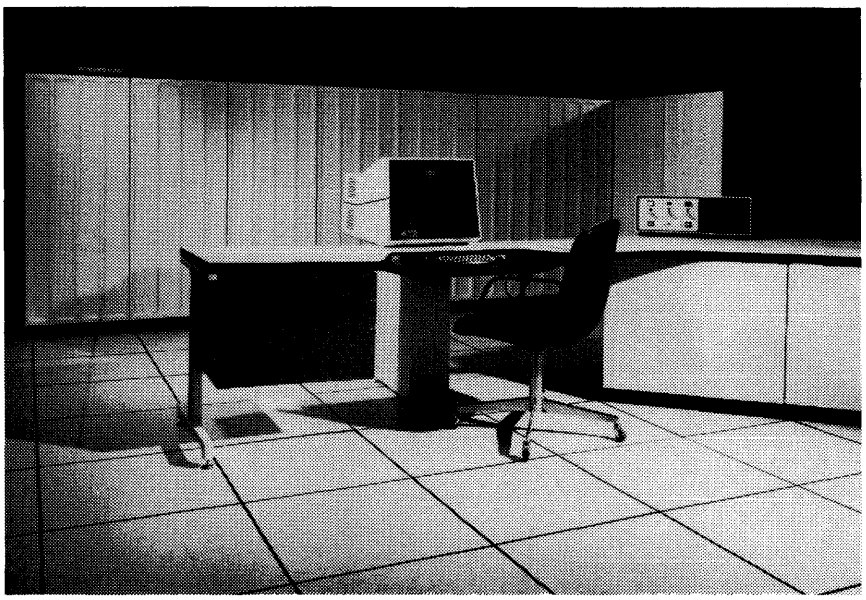
DATE OF FIRST DELIVERY: See characteristics chart.

NUMBER INSTALLED TO DATE: Over 500 worldwide.

DATA FORMATS

All data formats, instruction formats, and other architectural features completely follow IBM System/370 functional architecture.

BASIC UNIT: 8-bit bytes. Each byte can represent 1 alphanumeric character, 2 BCD digits, or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word." ➢



The Amdahl 470V/8, shown here, is the most powerful member in the 470 Series, with an execution rate of about 6.4 to 7.0 MIPS (million instructions per second). All 470 systems are air-cooled, and can execute any IBM System/370 software as well as utilize System/370-compatible peripheral devices.

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CHARACTERISTICS OF THE AMDAHL 470 SYSTEMS

	470V/7C	470V/7B
SYSTEM CHARACTERISTICS		
Relative performance	1.1	1.4 to 1.6
To	IBM 3033S	IBM 3032
Date announced	11/80	11/79
Date of first delivery	3rd Quarter 1981	3/80
Production status	Active	Active
Number of processors	1	1
Multiprocessor configurations	No	No
Principal operating systems	OS/VS1, SVS, MVT, MVS, MVS/SP, VM/370, VM/SP, ACP	OS/VS1, SVS, MVT, MVS, MVS/SP,VM/370, VM/SP, ACP
Upgradable to:	470V/7B	470V/7A
MAIN STORAGE		
Type	Dynamic NMOS	Dynamic NMOS
Cycle time, nanoseconds	320	320
Bytes fetched per cycle	4	4
Interleaving	8- or 16-way	8- or 16-way
Minimum capacity, megabytes	4	4
Maximum capacity, megabytes	16	16
Increment size (field upgrade)	4MB	4MB
Error detection and correction	8 bits/8 bytes	8 bits/8 bytes
PROCESSOR		
Cycle time, nanoseconds	29	29
Translation lookaside buffer	512 entries	512 entries
Segment table origin stack	128 entries	128 entries
Instruction lookahead	4 levels	4 levels
High speed buffer (Bipolar RAM)		
Cycle time, nanoseconds	58 for 4 bytes	58 for 4 bytes
Capacity, bytes	32K	32K
I/O Channels		
Number standard	8	8
Number optional	8	24
Subchannels per channel	256	256; opt. 512
Total subchannels	2,048	2,048; opt. 4,096
Channel to channel adapter	Yes	Yes
Block multiplexer, bytes per second	2.0M	2.0M
With two-byte interface	4.0M	4.0M
With data streaming	3.0M	3.0M
Selector, bytes per second	2.0M	2.0M
With two-byte interface	4.0M	4.0M
Byte multiplexer, bytes per second	110K	110K
Burst mode	2.0M	2.0M
Aggregate data rate, bytes per second	18M	18M

only about $500,000, compared to $532,000 and $639,000 for the 3033AP and MP, respectively. Those organizations requiring greater processing power than the 470V/8 should consider Amdahl's new 580 Series (Report 70C-044-03).

The Amdahl 470 configurations consist of a central processor unit with 8, 12, 16, 24, 28, or 32 integrated input/output channels, a minicomputer-based system console with CRT display, from 4 to 16 million bytes of main memory, and a power distribution unit. Central processor functions are performed by four independent functional units: a Storage Unit that controls accesses to main memory and includes both virtual address translation hardware and a cache memory; an Instruction Unit for controlling instruction interpretation and execution; an Execution Unit that performs the arithmetic, logic, and data manipulation functions of instruction execution; and a Channel Unit that interprets

FIXED-POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode.

FLOATING-POINT OPERANDS: 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short" format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; for 4 words in "extended precision" format.

INSTRUCTIONS: 2, 4, or 6 bytes in length, which usually specify 0, 1, or 2 memory addresses respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: Dynamic NMOS.

CYCLE TIME: See characteristics chart.

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CHARACTERISTICS OF THE AMDAHL 470 SYSTEMS

	470V/7A	470V/7	470V/8
SYSTEM CHARACTERISTICS			
Relative performance	1.0 to 1.1	1.0	1.1
To	IBM 3033N	IBM 3033U	IBM 3033U
Date announced	8/79	3/77	10/78
Date of first delivery	9/79	8/78	9/79
Production status	Active	Active	Active
Number of processors	1	1	1
Multiprocessor configurations	No	No	No
Principal operating systems	OS/VS1, SVS, MVT, MVS/SP, MVS, VM/370, VM/SP, ACP	OS/VS1, SVS, MVT, MVS/SP, MVS, VM/370, VM/SP, ACP	OS/VS1, SVS, MVT, MVS/SP, MVS, VM/370, VM/SP
Upgradable to:	470V/7	470V/8	—
MAIN STORAGE			
Type	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS
Cycle time, nanoseconds per 32 bytes	320	320	320
Bytes fetched per cycle	4	4	4
Interleaving	8- or 16-way	8- or 16-way	8- or 16-way
Minimum capacity, megabytes	4	4	4
Maximum capacity, megabytes	16	16	16
Increment size (field upgrade)	4MB	4MB	4MB
Error detection and correction	8 bits/8 bytes	8 bits/8 bytes	8 bits/8 bytes
PROCESSOR			
Cycle time, nanoseconds	29	29	26
Translation lookaside buffer	512 entries	512 entries	512 entries
Segment table origin stack	128 entries	128 entries	128 entries
Instruction lookahead	4 levels	4 levels	4 levels
High speed buffer			
Type	Bipolar RAM	Bipolar RAM	Bipolar RAM
Cycle time, nanoseconds	58 for 4 bytes	58 for 4 bytes	52 for 4 bytes
Capacity, bytes	32K	32K	64K
I/O Channels			
Number standard	12	12	12
Number optional	20	20	20
Subchannels per channel	256; opt. 512	256; opt. 512	256; opt. 512
Total subchannels	2,048; opt. 4,096	2,048; opt. 4,096	2,048; opt. 4,096
Channel to channel adapter	Yes	Yes	Yes
Block multiplexer, bytes per second	2.0M	2.0M	2.0M
With two-byte interface	4.0M	4.0M	4.0M
With data streaming	3.0M	3.0M	3.0M
Selector, bytes per second	2.0M	2.0M	2.0M
With two-byte interface	4.0M	4.0M	4.0M
Byte multiplexer, bytes per second	110K	110K	110K
Burst mode	2.0M	2.0M	2.0M
Aggregate data rate, bytes per second	18M	18M	18M

and executes input/output instructions and interfaces with the standard control unit interface that can communicate with any System/360- or System/370-compatible peripheral equipment. Operation of all the functional units can be overlapped, and 8- or 16-way interleaving can be performed on accesses to main memory. The degree of interleaving is partially dependent on the processor model.

Amdahl Corporation was the first company to develop and produce an IBM plug-compatible mainframe computer. The company was formed in 1971 by Dr. Gene Amdahl, principal designer of the IBM System/360 and subsequently a director of IBM's advanced systems laboratory and an IBM Fellow, the company's highest scientific position.

TECHNOLOGY

At the time when development began on the Amdahl 470, economically practical LSI technologies were not

CAPACITY: See characteristics chart. Memory units are equipped with their own power supply. Availability of expanded main memories up to 32 megabytes will be announced in the first quarter of 1982.

CHECKING: Error checking and correction (ECC) circuitry in main memory performs automatic correction of all single-bit errors and detection of all double-bit and most other multiple-bit memory errors. See table for number of bits per byte group added for ECC.

A Configuration Control Register, associated with each two-million-byte storage unit, maintains a map of the assignment of main storage address space for that storage unit. In the event of an unrecoverable memory error, the memory module can be removed from operation and the remaining memory reconfigured for continuous system operation. This process typically involves memory increments of two megabytes.

In addition, a parity check is performed on all data transferred between main memory and the High-Speed Buffer. A separate parity check is also made on storage keys,

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available to produce circuit chips with the density and speed required to implement the Amdahl concepts. As a result, all of the circuitry, plus the manufacturing techniques, test equipment, and chip interconnection methods, were designed by Amdahl engineers.

The LSI chips developed for the Amdahl 470 measure 154 thousandths of an inch square, are 10 mils thick, and have a maximum capacity of about 100 circuits. The LSI chips are mounted on a multiple-chip carrier, which is the field-replaceable unit of the system. Each carrier has a maximum capacity of about 4200 circuits. Thus, all circuits comprising the 470V/7 system can be housed on 61 multiple-chip carriers (MCCs), resulting in a system requiring much less floor space than a comparable IBM 3033 with its associated channels. The Amdahl circuits also require significantly less power than that consumed by standard TTL circuitry, resulting in significantly reduced cooling requirements for the system. All 470 systems are air-cooled, and a cooling stud is bonded to the surface of each LSI chip carrier to conduct heat into the air flow.

The miniaturization of the 470 circuitry substantially reduces the number of wiring interconnections required in the system, resulting in potentially fewer system failures. Additional circuitry on each subassembly also allows some 17,000 key logic points in the system to be examined and exercised by diagnostic programs under control of the system console. Remote diagnostic services are also available through a modem supplied with the system console. Other reliability features incorporated in the design include instruction retry, error checking and correction (ECC) circuitry in main memory, and the ability to recover from high-speed buffer and main memory failures by configuring out the malfunctioning portions of the buffer and main memory.

Although the basic concept underlying the 470 system design is to produce an extremely fast but architecturally simple computer system, sophisticated modifications have been made to several key functional components to achieve more efficient operation. The high-speed buffer, for example, uses a "non-store-through" technique, permitting data to be modified in the buffer without updating main storage. Main storage is updated only when the data is written back to main storage to provide space for new data. In addition, Amdahl has engineered a number of probe points into the hardware to facilitate the use of hardware monitors and has recently introduced a Hardware Measurement Interface (HMI). The HMI can be used with most commercial hardware monitors.

PROCESSORS AND MAIN MEMORY

The Amdahl 470 design is based on the System/370 functional architecture. It achieves its superior performance through the use of the latest in super-fast integrated circuit technology and, to a lesser extent, from central processor architectural optimization that provides for more efficient operation of the high-speed memory and the virtual-storage address translation hardware, and permits

which are used to implement storage protection and to record references and modifications to main storage.

STORAGE PROTECTION: Storage protection facilities are comparable to those implemented in the IBM System/370.

RESERVED STORAGE: The 470 processors reserve an area in lower memory for such purposes as interrupt handling routines, CPU ID, channel ID, and machine check logouts.

STORAGE CONTROL UNIT (S-UNIT): The Storage Control Unit. or S-Unit, handles all requests for data from main storage made by the CPU and the channels. An internal priority structure is used to resolve conflicts resulting from multiple concurrent requests for access to main memory. The internal priority structure of the S-Unit has the following five priority levels, in descending order: Internal High (including ECC handling), Channel Unit High, Central Processing Unit, Channel Unit Low, and Internal Unit Low (such as instruction prefetch). Normally, the central processor unit is given higher priority than a channel except when a channel issues a high-priority request. The Storage Control Unit locates the requested data either in the High-Speed Buffer or in main memory and includes a dynamic address translation facility for translating program-specified virtual addresses into real-memory addresses.

All Amdahl processors include a High-Speed Buffer (HSB) that is organized as a set associative memory composed of eight partitions. Each partition is organized into 32-byte lines that can be addressed on a single-word or double-word basis.

The 470V/7, 470V/7A, 470V/7B, and 470V/7C all have eight equal partitions with each partition having 128 32-byte lines. The 470V/8 is partitioned four ways where each partition has 512 32-byte lines. Partitioning allows the system to bypass buffer errors by reconfiguring out a buffer section. The 470V/8 HSB incorporates a special prefetching technique which predicts the next most logical consecutive data to be called into the buffer from main storage and then moves the data into the buffer.

For systems control programs using 2K pages, the HSB operates in 16K mode, causing each buffer partition to contain 64 32-byte lines.

Data is transferred between the buffer and the central processing unit in groups of 4 bytes per cycle and is brought into the buffer from main memory in lines of 32 bytes, each requiring 4 buffer cycles. In contrast to the System/370, Amdahl I/O channels as well as the CPU access the High-Speed Buffer. A tag field associated with each 32-byte line in the buffer includes a block identifier containing the high-order real address bits of the buffer data, plus parity and check fields, modification indicators, and reference bits to specify whether a central processor or channel access brought the data into the buffer and whether the CPU was in the supervisor or problem state of operation.

When a request is made for data by the central processor Instruction Unit or by the Channel Unit, the Storage Control Unit forms a pointer into the buffer and reads a 32-byte line of data from each partition of the buffer. The S-Unit then uses the real line address calculated by the address translation hardware to select one of the lines, and a tag comparison on the real address bits is used to select the data from the proper partition of the buffer. Location of the data in the buffer can be performed in two machine cycles, although overlapped buffer operations allow it to accept a request for data during each cycle. If the data is not in the buffer, a main storage request is generated and the request data is made available to the program and is also placed in the High-Speed Buffer.

Operation of the High-Speed Buffer is based on a non-store-through technique, in which data that is modified in the buffer

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extensive overlapping of input/output operations and instruction execution in the central processor.

Large-scale integrated (LSI) semiconductor circuits are used extensively throughout the system, resulting in increased processing speeds, higher reliability, and reduced space and cooling requirements. The central processor uses an LSI version of bipolar emitter-coupled logic (ECL) with chip speeds in the area of 600 picoseconds (trillionths of a second), and has a CPU cycle time of 29 nanoseconds for the 470V/7 systems, while the 470V/8 boasts a cycle time of 26 nanoseconds.

Instruction execution is performed in a "pipeline" structure which allows the execution of various phases of up to six instructions to occur concurrently within the pipeline. This results in a maximum execution rate of one instruction per two processor cycles. In addition, although the Amdahl Dynamic Address Translation (DAT) feature provides virtual-storage operations comparable to those of the System/370, Amdahl has extended its design for more efficient operation. The Amdahl DAT feature maintains a segment table origin (STO) stack that allows up to 128 different virtual-storage environments to maintain translation information in the Translation Lookaside Buffer, reducing the amount of updating activity in the buffer.

When the capacity of the STO stack is exceeded, the oldest entry in the stack and its associated translation lookaside buffer entries are purged during spare machine cycles. In the 470V/7 series and 470V/8, the translation lookaside buffer portion of the address translation hardware has also been expanded to 512 entries, compared to the System/370's 128.

Main memory in the 470 processors is metal oxide semiconductor (MOS) LSI circuits with a cycle time of 320 nanoseconds (depending on processor model). Ultra-high speed components are used in the cache-like buffer memory with a 52 (470V/8) or 58 (470V/7 series) nanosecond cycle time per up to 8-byte access. Buffer loading from main memory is performed in 32-byte blocks. Memory interleaving can be either 8-way or 16-way.

INPUT/OUTPUT CONTROL

The Amdahl 470 systems are equipped initially with either 8 (470V/7A, V/7B and V/7C) or 12 (470, V/7 and V/8) high-speed channels. All 470 models can be expanded to 16 channels, and, in the second quarter of 1981, to 32 channels (except the 470V/7C). Each I/O channel can be configured as a byte multiplexer, a block multiplexer, or a selector channel. Byte multiplexer channels have a maximum data transfer rate of 110,000 bytes per second. Block multiplexers and selectors can transfer data at 2 million bytes per second, or at 4 million bytes per second using the optional two-byte interface. The 3 million-bytes-per-second data streaming feature will be available for any two channels within a four-channel group starting in the

is not written to main storage until the line is removed from the buffer to make room for new data. As a result, frequently referenced data can be accessed and modified in the buffer without incurring a large number of main memory accesses. An instruction prefetch function can be enabled for accesses to the buffer from input/output channels, the operand stream, or the instruction stream. A combination of three bits in the Storage Unit controls the order of prefetch operations, although that order can be modified through the use of an additional register bit provided for that purpose. Six operating state register bits are used to control the operation of the buffer replacement algorithm. Four additional bits of the S-Unit operating state register can be set through the System Console, and can be used to partition the buffer to configure out a portion of the buffer with a hardware failure.

DYNAMIC ADDRESS TRANSLATION: The dynamic address translation facility is located in the S-Unit. It controls the translation of program-specified virtual addresses into real-memory addresses when the 470 is operating in extended control (EC) mode. Virtual memory implementation in the 470Vs is similar to that of the IBM System/370. Virtual storage is divided logically into segments of 64K bytes or 1024K bytes, which are in turn divided into pages of either 2048 or 4096 bytes. Segment and page tables are maintained in main storage to perform address mapping. A high-speed Translation Lookaside Buffer (TLB) is used to store the most recently referenced addresses, and a Segment Table Origin (STO) stack stores information on the size and main memory location of the segment table associated with TLB entries.

The STO stack contains 120 locations, and is addressed by the current segment table origin. The TLB is divided into primary and alternate halves, each containing 256 address pairs.

Translation of virtual to real addresses for data located in the TLB is overlapped with the High-Speed Buffer search, and data for both real and virtual operation can be accessed in two S-Unit cycles. If the data is not located in the TLB, an address translation is performed and two additional storage references are required to locate the data either in High-Speed Buffer or in main memory. The new translated address is translated in the TLB acording to an algorithm similar to that used by the High-Speed Buffer.

The STO stack contains virtual-storage identification fields associated with the TLB entries. The identification fields correspond with address translation information such as segment table size and location, contained in Control Register 0 and Control Register 1. When the contents of these registers are modified, subsequent TLB entries are assigned a new STO ID by the S-Unit, but earlier TLB entries are not invalidated provided they do not exceed the capacity of the stack. If Control Registers 0 and 1 are restored to a previous value, any previous TLB entries remaining are thus still available. The S-Unit controls selective purging (when an STO entry is automatically removed from the stack and its associated TLB entries invalidated) of the TLB and STO stack during spare cycles.

CENTRAL PROCESSOR

Central processor functions such as instruction fetching and decoding and instruction execution are performed by two separate units, the Instruction Unit (I-Unit) and Execution Unit (E-Unit).

The I-Unit controls instruction execution through a pipeline structure and can have up to six instructions concurrently in some phase of execution. The instruction execution process is divided into the fetch phase plus six additional decoding and execution phases. The instruction fetching operation requires three cycles, while Phases A, B, and C, which perform instruction decoding, operand address generation, and operand retrieval, each require a minimum of two central

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third quarter of 1981. A 470 system can have from 2 to 8 data streaming channels, depending on the processor model. The aggregate data rate, however, is the limiting factor in each system, and this, in turn, is governed by the channel-to-processor interface circuitry of each four-channel group. The exact aggregate data rate is heavily dependent on the system configuration, but a rule-of-thumb value is available. The aggregate data rate is approximately 18 million bytes per second on 470V/7 series and 470V/8 systems.

A dynamic priority allocation scheme based on the availability of space in each channel buffer is used to allocate cycles between central processor operations and input/output data transfers. Normally, the central processor has the highest priority in the system, but channels performing high-speed data transfers are allowed to take precedence over the central processor by the Amdahl internal priority scheme. This allows high-speed devices to be attached to any channel without performance degradation and provides additional flexibility in the configuration of peripheral subsystems.

COMMUNICATIONS CONTROL

Amdahl's new 4705 Communications Processor, unveiled last October, is program-compatible with IBM's 3705-II and is said to have 1.8 times its throughput.

The new controller has 64K bytes of memory, and is expandable to 512K in 64K-byte increments. Up to 352 communications lines can be connected to the 4705, with transmission speeds up to 56,000 bps possible. As many as four CPUs can be connected to a 4705 through a special adapter. Host channels can be either byte multiplexer, block multiplexer, or selector-type.

Communications features include support for the following access methods—BTAM, QTAM, TCAM, VTAM, ACF, and MSNF. The 4705 is compatible with IBM's SNA network architecture and handles the following protocols: BSC, SDLC, and start/stop. Communications lines can have the following characteristics: half- or full-duplex, EIA RS-232-C and CCITT V.24 and V.35.

The 4705 also features on-line and stand-alone diagnostics, instruction lookahead, instruction retry, and automatic fault isolation. Deliveries began in November, 1980.

COMPETITIVE POSITION

Amdahl targets its 470 models against specific IBM 303X processors, which is characteristic of the PCM industry. The new entry-level 470V/7C was announced a week later than, and has about 10 percent more performance than the IBM 3033 Model Group S. The 470V/7B is about 40-50 percent more powerful than the 3032. The 470V/7A and 470V/7 are about 10 percent more powerful than 3033N and 3033U, respectively. The 470V/8 has about 25-30 percent more power than the 3033U, according to

processor cycles. Phases D, E, and F each require a minimum of one cycle, and perform execution plus checking and writing of the results of the instruction execution. The overlapped instruction execution in the pipeline can result in the completion of an instruction execution every two machine cycles, except in the case of long instructions requiring additional cycles for execution.

Extensive parity checking is performed throughout the I-Unit. All incoming instructions are checked for parity, and the results are checked again after the completion of execution. All control registers and the program status word are checked each time they are used. In addition, parity is checked for the timer and the address generation function, and parity is also maintained for all program-referable data.

The Execution Unit (E-Unit) executes arithmetic and logical instructions received from the I-Unit; it consists of a logical unit and checker (LUCK), a group of functional units (multiplier, adder, shifter, and byte mover), a table lookup unit to generate an inverse in the I-register (for divide operations), registers for storage of intermediate results, and a result register for output of the result of instruction execution to the I-Unit. Instruction operation codes plus control information are sent from the I-Unit to the E-Unit, and instruction operands are received either from the I-Unit or directly from main storage. The LUCK checks the validity of incoming operands, performs logical operations and comparisons on incoming operands, validates decimal digit formats, sets conditions codes, and counts leading zeroes for use in shifting and normalization. LUCK operations require one CPU cycle. Additional arithmetic functions are performed by the multiplier, adder, shifter, and byte mover units, each of which also completes its functions in one machine cycle.

When instructions require processing by multiple E-Unit functions, the I-Unit synchronizes the operation of its pipeline by delaying the progress of other instructions in the pipeline until the final cycle of the instruction that is currently in the E-Unit. The E-Unit performs parity checks on all incoming data and on logical and shift operations, and uses a check summation technique to verify the results of addition and multiply functions. The E-Unit also generates parity for final instruction execution results, and the parity is checked by the I-Unit before storing the final results.

Failure to complete the execution of an instruction because of a hardware malfunction results in a machine check condition. Most instructions in the Amdahl 470 repertoire can be automatically retried by the E-Unit. The instruction retry feature attempts to re-execute the failed instruction (in contrast to returning the machine state to a hardware checkpoint). Instructions that cannot be retried or recovered result in a hard machine check, which is handled according to standard System/370 procedures.

The Amdahl 470 family uses a "fourth-generation" LSI packaging technique that was developed to reduce both physical system size and power consumption. The basic logic unit of the 470 system is a "chip" that contains 75 to 100 emitter-coupled logic (ECL) circuits and requires significantly less power. Each chip has its own air cooling fins. The chips are mounted in multiple chip carriers (MCCs) that can contain up to 42 of the LSI circuits. The MCCs are, in turn, connected to a computer backplane with the chip cooling fins protruding into an air stream. The 470V/7s and the 470V/8 contain 59 MCCs. The use of air cooling in the 470 systems is a distinct advantage over their IBM counterparts, the System/370-168 and the 3033.

PROCESSOR FEATURES: The standard timing features of the System/370 architecture are included in all Amdahl central processors. These include a CPU timer and a Clock

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Amdahl. Beyond the 470V/8, you should consider Amdahl's new 580 Series (Report 70C-044-03). Amdahl's pricing activities usually mirror those of IBM, in addition to matching IBM's products stride-for-stride.

One aspect of the IBM 3033 that could have caused trouble for Amdahl was IBM's increased use of system-level microcoding in the 303X, such as that used in the 3033 Extension Feature. This technique goes beyond the implementation of the basic instructions in microcode and adds frequently-used operating system functions to the 303X's firmware complement. By implementing portions of the operating system in firmware, IBM tried to make it difficult for the new MVS/SE (and, lately, MVS/SP) enhancement program product for its MVS operating system to be executed in Amdahl systems. Amdahl responded with the development of a software solution to the problem known as MVS/SE Assist. As IBM makes additional MVS updates, Amdahl plans to meet them head-on with upgraded MVS/SE packages.

SOFTWARE AND SUPPORT

Amdahl maintains a Software Systems Support group in Sunnyvale, California that supplies its own versions of the supported IBM Systems releases. Supported operating system software includes OS/VS1, SVS, MVS, MVT, VM/370, and ACP. Amdahl will also support VM/SP and all MVS/SP releases as they become available. IBM subsystems such as TSO, TCAM, JES2, JES3, VTAM, RSCS, CMS, and IPCS are also supported. Amdahl-developed software includes VM/PE and VM/SA, which allow a user to get increased performance from MVS or SVS when running VM/370; the previously mentioned MVS/SE Assist; MVS/SE Support, similar to MVS/SEA, which is designed for IBM 370/158 and 370/168 MP and AP versions; VM/ECS (Extended Channel Support) and MVS/ECS, which can support up to 32 I/O channels in a 470; UTS (Universal Timesharing System), based on the UNIX operating system; IMS/VS HDAM Optimizer, designed to improve the performance of the IMS/VS data base management system; and ACP/System Error Dump Analysis, for formatting on-line ACP memory dumps.

IMS/VS HDAM Optimizer was the first Amdahl Internally Developed Software (AIDS) product. AIDS products are being designed to improve system performance and productivity of the DP staff, but are developed and supported by individuals and are distributed on an as is basis with no warranty.

USER REACTION

Datapro's 1981 Computer Survey produced responses from 27 Amdahl users, representing a total of 38 installed systems. A total of 29 systems were actually rated. Seventeen users had single systems, nine had two units in place, and one Amdahl user had three systems running. The models represented were fairly evenly divided: 470V/5—3, 470V6—7, 470V/6-II—7, 470V/7—4, 470V/8—7, and one unnamed system. The newest system

Comparator; the latter provides a means for causing an interrupt when the standard Time-of-Day Clock reaches a program-specified value. Additional instructions are provided to set and store the Time-of-Day Clock, Clock Comparator, and CPU Timer.

Other features of the System/370 found in Amdahl processors include control registers, direct addressing, double word buffer, interval timer, machine check handling, multiple bus architecture, time-of-day clock, channel command retry, channel indirect addressing, byte-oriented operand feaure, console audible alarm, remote console, remote data link, console file, extended control mode, and program event recording. Control registers are used for operating system control of relocation, priority interruption, program event recording, error recovery, and masking operations. A double-word buffer consists of a 64-bit area temporarily reserved for data used in performing an I/O operation. Each channel attached to the CPU has a fixed amount of channel control buffer dedicated to its use.

The interval timer is a 32-bit decremental counter that is reduced by one several hundred times per second. The timer generates an interrupt when the contained value is decremented from a positive to a negative number. Machine check handling analyzes errors and attempts recovery by retrying the failed instruction if possible. If retry is unsuccessful, it attempts to correct the malfunction or to isolate the affected task. Multiple bus architecture implies that the various segments of the processor, namely memory, arithmetic and logic, central control, etc, are tied together by more than one central bus. The time-of-day clock is incremented once every microsecond and provides a consistent measure of elapsed time suitable for the indication of date and time. Some channels have the capability to perform channel command retry, a channel and control-unit procedure that causes a command to be retried without requiring an I/O interrupt. Channel Indirect Addressing (CIA) is a companion feature to dynamic address translation, providing data addresses for I/O operations. CIA permits a single channel command word to control the transmission of data that crosses noncontiguous pages in real main storage. If CIA is not indicated, then channel one-level (direct) addressing is employed.

The byte-oriented operand feature permits storage operands of most non-privileged operations to appear on any byte boundary. Instructions must appear on even byte addresses. The console audible alarm is a device activated when predetermined events occur that require operator attention or intervention for system operation. A remote console is a console attached to a system through a data link. The remote console is configured in addition to the standard console. The remote data link allows establishment of communications with a technical data center to remotely diagnose system malfunctions. The console file is the basic microprogram loading device for the system, containing a read-only file device. The media read by this device contains all the microcode for field engineering device diagnostics, basic system features, and any optional system features. The extended control mode (EC) is a mode in which all features of the System/370 computing system, including dynamic address translation, are operational. Program event recording is a hardware feature used to assist in debugging programs by detecting and recording program events.

The Direct Control Feature, as on the System/370, provides six external interrupt lines which operate independently of the normal data channels, plus the Read Direct and Write Direct Instructions which provide for single-byte data transfers between an external device and main storage.

The optional Channel-to-Channel Adapter permits direct communication between an Amdahl processor and a

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was installed in January of this year, the oldest was installed October, 1975, and the average age was just over two years.

Twenty-five systems replaced a previous machine, and four were new installations. Of the systems replaced, the most frequently reported were large-scale IBM System/370 and 303X processors. One user upgraded an older Amdahl processor to a newer one.

The business types represented most frequently were banking and government (a tie), followed by manufacturing and education (another tie). There was a three-way tie for third place among insurance firms, service bureaus, and public utilities. Of the applications reported by these firms, the most frequently reported was accounting/finance (21 responses), followed closely by payroll/personnel (17 responses), purchasing (13 responses), and order processing/inventory control (11 responses). Every respondent developed some or all of his applications in-house, about half used contract programming or bought proprietary software, and the rest obtained applications from the manufacturer.

Each Amdahl processor was installed at a central site, typical of a large-scale mainframe. Nineteen users reported distributed processing locations of anywhere from one to over ten nodes; seven indicated they had no distributed processing sites. All firms reported local and/or remote terminals, and the majority of users said they had over 60 terminals of each type. Memory size was divided between four to eight megabytes (14 responses) and over eight megabytes (15 responses). Just about every user had over 1.2 gigabytes of on-line disk storage, with only five reporting less than that capacity.

By far the most widely used operating system was MVS, with 24 responses. Use of a data base management system (DBMS) was reported by all users except one, and all respondents were running some sort of communications monitor. The most widely used program language was COBOL (23 responses), followed by Assembler, FORTRAN, and PL/1. Only five users said they were running any word processing on their Amdahl systems.

Amdahl users have ambitious plans for their operations in 1981. Twenty said they were looking to add more hardware and proprietary software, 19 are planning more data communications, 16 want to increase their distributed processing activities, and 12 plan to acquire more manufacturer's software. Five said they were going to perform more word processing, and 2 said they were planning to add another Amdahl processor this year.

That Amdahl users are pleased with their systems is quite clear as 24 users had no plans to replace their systems in 1981. Those who were planning on a replacement were evenly divided between Amdahl and other vendors. In spite of this, every user said his Amdahl system performed up to his expectations, and, with only one exception (he

System/370, 303X, or 3081 via a standard I/O channel. It can be attached to either a selector channel or a block multiplexer channel and uses one control unit position on either channel. In a loosely-coupled configuration consisting of an Amdahl 470 and a System/370, 303X, or 3081, either system can be equipped with the Channel-to-Channel Adapter, and it is required on only one of the interconnected channels.

The Two-Byte Interface, available as an option for all selector and multiplexer channels, doubles the bandwidth of the data path between the channel and the control units which support this option.

The Data Streaming feature, which permits data transfer rates of 3 megabytes per second, was announced for all Amdahl processors on August 4, 1980. In any given four-channel group, up to two channels can be designated as high-speed. Within the 470V/7 and 470V/8 product lines the number of data streaming channels ranges from two to eight.

The maximum number of channels in the 470V/7 and 470V/8 systems (except the 470V/7C) was increased to 32 in a September, 1980 announcement. Once the initial 16 channels are in place, expansion to 32 progresses through one 8-channel and two 4-channel increments. The maximum number of subchannels was also doubled, from 2,048 to 4,096.

OPERATIONAL MODES: Like the System/370, the Amdahl CPUs can operate in either the Basic Control (BC) or Extended Control (EC) mode. The BC mode maintains general upward compatibility with the System/360 architecture and programming. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other new system control functions; therefore, the virtual-storage-oriented operating systems must be used.

REGISTERS: Sixteen 32-bit general registers are used for indexing, base addressing, and as accumulators. Other program-visible registers are the same as in the System/370. Machine-dependent registers contained in the 470 processors are not visible to the user and may differ from the System/370.

ADDRESSING: The same techniques as employed in the System/370 and 303X are found in the 470 processors.

INSTRUCTION REPERTOIRE: The Amdahl 470 instruction set consists of the complete System/370 Universal Instruction Set, including the five System/370 instructions for Dynamic Address Translation. Two exceptions are the Store CPU ID (STIDI) and Store Channel ID (STIDC) instructions, which differ in their operations because of architectural differences between the System/370 and the Amdahl processors. In the Amdahl units, a machine check extended logout (MCEL) is performed by the Console Processor in its own memory, whereas in the System/370 the address in main memory and size of the machine check extended logout are dependent on the central processor model and control register information. Since the MCEL on the 470 is made to the Console Processor, the MCEL length field stored by the STIDP instruction is all zeroes. The model number is 0470. The STIDC instruction stores zeroes for a channel model number because all Amdahl channel types are implicit in CPU type. According to Amdahl, no system or application program is likely to be affected by these model dependencies.

INSTRUCTION TIMING: The following instruction execution times, in nanoseconds, have been estimated by scaling performance information supplied by Amdahl for the Model 470V/6 in the absence of specific timing data for the

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was undecided), would recommend Amdahl to another prospective user.

The following chart summarizes how these Amdahl users felt about their systems.

	Excellent	Good	Fair	Poor	WA*
Ease of operation	13	14	2	0	3.4
Reliability of Mainframe	17	12	0	0	3.6
Reliability of Peripherals	5	20	3	0	3.1
Responsiveness of maintenance service	18	11	0	0	3.6
Effectiveness of maintenance service	12	13	4	0	3.3
Technical support:					
Trouble-shooting	9	17	3	0	3.2
Education	8	15	5	1	3.0
Documentation	5	21	1	1	3.1
Operating system	4	18	1	0	3.1
Compilers and assemblers	4	16	0	0	3.2
Applications programs	2	12	1	0	3.1
Ease of programing	5	16	1	0	3.2
Ease of conversion	10	14	1	0	3.4
Overall satisfaction	6	22	1	0	3.2

*Weighted Average on a scale of 4.0 for Excellent.

Datapro telephoned several Amdahl 470 users around the country for their comments. We noted a number of similarities among Amdahl users, particularly concerning Amdahl service, and their relationships with IBM.

We first called on a northeastern financial institution that has a mixed shop, with both IBM and Amdahl systems operating. Due to prolonged delays in obtaining a second System/370-158, they decided on an Amdahl 470V/5. It was installed 30 days after the contracts were signed. It was subsequently upgraded to its present level, a 470V/6-II, and handles check processing, CICS, and all batch operations. The original 370/158 is used for TSO. The Amdahl's uptime is "never under 99%," and "the worst was 99.3%." Things were not so good at the start, according to the DP manager. Amdahl's field support staff had some initial difficulties but quickly turned the situation around. Today Amdahl takes a very aggressive position, and he considers them "very responsive" to their needs. Currently the 470V/6-II is scheduled to be upgraded later this year. The contestants are to be the 470V/8 and the IBM 3033. The DP manager told Datapro he believes it's "a good idea to have one of each system." Overall he was very pleased with his Amdahl 470.

Another satisfied Amdahl user was a midwestern insurance firm that is also a two-vendor shop. At their headquarters they currently have a 470V/6-II, a 470V/7A, and an IBM 370/168AP. The 470V/7A is being upgraded to a 470V/8, and an IBM 3033 is on order. When their new corporate data center is completed in about two years, they will probably have Amdahl and IBM systems there, side-by-side. The firm's DP manager told us a new IBM 3081 is on order, and they are close to making a decision on an Amdahl 580. Uptime on both Amdahl systems is "nothing short of incredible." When Amdahl entered the picture, IBM withdrew a lot of its support, causing some hectic

newer models. Timings are presented for the 470V/6-II, 470V/7, and 470V/8 as representative systems.

	470V/6-II	470V/7	470V/8
Add (32-bit binary):	65	40	32
Multiply (32-bit binary):	228	140	112
Divide (32-bit binary):	1625	1015	812
Load (32-bit binary):	65	40	32
Store (32-bit binary):	65	40	32
Add (5-digit packed decimal):	423	265	212
Compare (5-digit packed decimal):	488	305	244
Add (short floating-point):	195	120	96
Multiply (short floating-point):	260	165	132
Divide (short floating-point):	878	550	440
Add (long floating-point):	260	165	132
Multiply (long floating-point):	650	405	324
Divide (long floating-point):	2080	1300	1040

PHYSICAL SPECIFICATIONS: Environmental conditions for 470 processors is given in the following table.

	Operating
Temperature Range	60° to 90° F
Optimum Temperature	75° F
Relative Humidity Range (noncondensing)	35% to 55%
Optimum Relative Humidity (noncondensing)	50%
Maximum Wet Bulb Temperature	78° F
Maximum Altitude (feet equivalent pressure)	+7,000

The Amdahl 470 processors are air-cooled and require a minimum of 12.5 tons of air conditioning and 4890 cubic feet of air per minute. Minimum BTU output for a 470 processor is 79,000 BTUs per hour. Figures are generally higher depending on the processor model and amount of memory installed. Power must be available to the Amdahl 470 power distribution unit from two sources, 415 and 60 Hz. Both sources must be four wire and three phase at 208 volts.

The processors in the upper end of the 470 line, including the 470V/7, are 72 inches long, 64.5 inches high, 30 inches wide, and weigh 6,800 pounds in a 12-megabyte, 12-channel configuration.

A typical configuration layout requires a 200 by 154 or 220 by 30 inch area depending on the layout (exclusive of the console). The console requires a 173 by 113 inch area.

CONSOLE INPUT/OUTPUT

The system console includes a minicomputer that acts as a console processor, an operator control panel, and a 3200-character CRT display and keyboard. The console processor is also equipped with a magnetic disk cartridge that is used by the console operating system and for logout and other functions, a floppy disk unit for loading diagnostic programs, and a modem to provide for remote diagnostic services.

The console has a direct interface to the central processing unit to allow access to the status of approximately 17,000 system key logic points and setting of control and data registers. The computer-to-console interface allows diagnostic tests to be performed on the central processor modules under control of the Console Processor without regard to the operating condition of the central processor, the

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moments. Things eventually were worked out, and both vendors have their systems running smoothly. The DP manager told us his two-vendor shop had its rough moments, but he feels the arrangement has been beneficial to his firm.

Moving to the southwest, we called on two firms—a multi-location, multi-vendor service bureau, and an "Amdahl-only" financial organization. The service bureau has three processing centers in their headquarters city alone, and runs four Amdahl 470V/8s and three IBM 3033s. The financial firm has an Amdahl 470V/6 and a 470V/7, which will be converted to a V/8 shortly. Both firms have Amdahl 580s in their plans. The service bureau's DP manager told us he has some IBM 308 1s on order, and was placed high up on the waiting list, a factor he figures might be due to Amdahl's presence. The service bureau bought Amdahl because of 1) cost and 2) they wanted to get away from a single-vendor arrangement, a decision that has proven to be a good one. Availability of a system quickly motivated the financial company to go Amdahl. Both DP managers had initial support problems with Amdahl, which were quickly corrected. They are very pleased with their Amdahl systems, regardless of being a one- or two-vendor shop. The service bureau's manager told us his uptime is "about the same as IBM," but Amdahl's "recoverability is better that IBM's." Typically achieving 99+% uptime on his two 470s, the financial company's manager added that using Amdahl's MVS/SE Assist program product "makes all the difference in the world."

Our final call was to a government organization in the northwest operating very successfully with a 470V/5. It replaced an IBM 370/155, and was chosen because of the cost, upgrade capability, and use of air-cooling. Uptime is typically 99% and better, and Amdahl's service currently is "excellent." The DP manager told us he also had initial support problems with Amdahl, but wasn't too upset, since IBM's support at the time was not that good, either. He felt that IBM's attitude was a result of being a single-processor site. Amdahl, on the other hand, is "aggressive." The firm is currently running two Software AG packages, Com-plete, and ADABAS, and has had no problems running them on the 470V/5.□

I/O channels, or other components of the main system. The system console is also equipped with a channel interface to a selector or multiplexer channel for operation as a standard console device.

The system console operates in three modes: the maintenance mode, the hardware command mode, and the device support mode. In the device support mode, the console emulates either an IBM 3066 system console or an IBM 3215 console printer-keyboard (using the CRT display for output in place of the 3210 matrix printers) and can be connected to either a selector or block multiplexer channel. Functions that can be performed in the hardware command mode include IPL, reset operations, display and modification of the contents of registers and main storage locations, and setting of operating conditions for the system.

INPUT/OUTPUT CONTROL

Each 470 central processor includes standard input/output channels, each of which can be configured as a byte multiplexer, block multiplexer, or selector channel. Data rates are given in the table on pages 01b and 01c.

The aggregate I/O data transfer rate for each system is less than the total of the maximum rates of all the attached channels. Each group of four channels shares certain hardware elements, causing contentions at the interface to the CPU.

Each selector-type channel can address up to 256 input/output devices and contains a single implicit channel for addressing one device at a time at burst-mode speeds. In the 470V/7C through 470V/7, 2,048 subchannels are available for assignment to either byte or block multiplexer channels. Channels with either 64 or 128 assigned subchannels can be configured for shared-channel operation. In channels with 64 subchannels, 4 can be shared, while those with 128 subchannels can have 8 shared subchannels. For the 470V/7 Series and 470V/8, subchannels are allocated in groups of 32, providing a total of 2,048 subchannels. The 470 Extended Channels option, available on all current models except the 470V/7C, increases the maximum number of subchannels to 4,096.

In all 470 processors, input/output operations are performed under control of the Channel Unit (C-Unit), which operates independently of central processor operations. the C-Unit consists of three major functional units called the Central Interface Control Logic (CICL), the Direct Access Control Logic (DACL), and the Operation Control Logic (OCL), plus buffers and communications areas and the Remote Interface Logic which interfaces to control units for any System/360 or System/370-compatible peripheral devices.

The CICL controls the transfer and buffering of data between the Channel Buffer Store and the peripheral devices. It polls the channels every eight cycles for data transfer requests, and transfers data from the Channel Buffer Store to the Remote Interface Logic one or two bytes at a time.

The DACL controls the movement of data between the Storage Unit and the Channel Buffer Store and has a data transfer rate of one word every eight cycles. The DACL is organized as a pipeline to allow overlapping of the functions. It polls each channel every 16 cycles for service requests, concurrently transfers data in both directions between the Storage Unit and the Channel Buffer Store, and reads or stores the results of each transfer operation.

The OCL translates channel commands and coordinates channel program execution for the C-Unit.

A dynamic priority scheme controls the allocation of service to I/O channels. Channels can issue high-priority and low-priority requests for service. Each channel is assigned a 32-byte buffer area in the Channel Buffer Store. Channels with less than half a buffer area remaining are assigned high priority, while those with more than half a buffer space available are assigned low priority. The S-Unit resolves conflicts for access to the High-Speed Buffer according to its own internal priority structure, permitting high-priority channel requests to take precedence over central processor requests for access to the High-Speed Buffer. An I/O operation is always executed at a higher priority than buffer prefetch operations.

The C-Unit performs parity checks on all input and output data transfers and on data transfers to the Storage Unit. Other functions include channel indirect addressing comparable to that implemented on the System/370 and 303X, and extended channel logout.

SIMULTANEOUS OPERATIONS: The Channel Unit operates independently of central processor operations. Both can access the HSB simultaneously and independently. Also,

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instruction lookahead is on four levels with a maximum of six instructions in the pipeline running concurrently with instruction execution, checking, and storage of results.

HARDWARE MONITOR INTERFACE: HMI is designed for customers who wish to monitor their 470V/7C, 470V/7B, 470V/7A, 470V/7, and 470V/8 processors, allowing users to record up to 30 categories of signals. The HMI does not record the signals, but makes them available so that they can be utilized by hardware monitors. The types of signals processed include quantity of instructions executed, processor time in active state, processor time in problem state, number of interrupts, and channel busy time. The HMI uses electronic buffering to protect the system from hardware monitor malfunctions and user errors. A set of HMI diagnostic instructions allows user access under software control.

AMDAHL DIAGNOSTIC ASSISTANCE CENTER (AMDAC): Located at Sunnyvale, CA, Columbia, MD, Toronto, and London, AMDAC is maintained 24 hours per day and 7 days a week by technical support specialists to solve difficult problems that cannot be resolved by field engineering on site. Via the modem in the user's 470 console, an on-line telephone hookup can be established between AMDAC and the customer system. AMDAC maintains a variety of system consoles, any of which can perform standard diagnostic tests on the user's system.

The scan circuitry can examine or reset the logic status of any one of the circuits being monitored, providing the capability to completely test and set all latches within the system. Scanning of latch points within the processing logic can occur even if the CPU is inoperative. When a failure occurs, internal logic information is displayed on the console CRT.

470/ACCELERATOR: Available in the 470V/7C, 470V/7B, and 470V/7A, the 470/Accelerator is a hardware product initiated by a software command. The feature is implemented in LSI circuitry within the 470 mainframe, and requires no additional cabinets or frames. The 470/Accelerator is designed for users who want increased processing power on an as-needed basis, without having expensive idle capacity over the long term. By invoking the 470/Accelerator, a 470V/7C user can have the power of a 470V/7B; a 470V/7B user the power of the 470V/7A; and the 470V/7A user the power of the 470V/7. Activation of the 470/Accelerator is by a single console command, ACCL. The feature is deactivated by the DECL command. 470/Accelerator billing is on a metered-hour basis.

470/EXTENDED PERFORMANCE ACCELERATOR: Similar to the 470/Accelerator, and also charged on an hourly basis, this feature is available only on the 470V/7B system and increases performance by 50 percent, equivalent to that of the 470V/7. Both features can be installed on a 470V/7B, and are mutually exclusive.

PERIPHERAL EQUIPMENT

The Amdahl 470 systems can utilize all IBM System/360 and System/370 input/output and mass storage devices, as well as their plug-compatible counterparts from independent vendors. Detailed coverage of many of these peripherals can be found in Volume 2 of DATAPRO 70.

COMMUNICATIONS EQUIPMENT

Amdahl's new 4705 Communications Processor, announced in October, 1980, is program-compatible with IBM's 3705-II front-end processor, and is claimed to have up to 1.8 times the throughput of a comparable 3705-II.

The new controller has 64K bytes of memory, and is expandable to 512K in 64K-byte increments. Up to 352 communications lines can be connected to the 4705, with transmission speeds up to 56,000 bps possible. As many as four CPUs can be connected to a 4705 through a special adapter. Host channels can be either byte multiplexer, block multiplexer, or selector-type.

Communications features include support for the following access methods--BTAM, QTAM, TCAM, VTAM, ACF, and MSNF. The 4705 is compatible with IBM's SNA network architecture and handles the following protocols: BSC, SDLC, and start/stop. Communications lines can have the following characteristics: half- or full-duplex, EIA RS-232-C and CCITT V.24 and V.35.

The 4705 also features on-line and stand-alone diagnostics, instruction lookahead, instruction retry, and automatic fault isolation. The system is scheduled for deliveries beginning in November 1980. For more details on the 4705, please refer to Report C13-044-101 in Datapro's Data Communications service.

SOFTWARE

Amdahl offers complete functional compatibility with IBM 360/370/303X software. Amdahl Corporation intends to support users of current IBM system software by providing new releases of the software to Amdahl users, including minor modifications to account for differences in the way the 470s handle machine check conditions, and by supplying software support services for its customers. Modifications are analogous to installing different models of the operating system on System/370 processors. Operating systems supported include OS/VS1, SVS, MVS, MVS/SP, MVT, VM/370, VM/SP, and ACP. Support is included for such major IBM subsystems as HASP, ASP, TSO, TCAM, JES2, JES3, VTAM, RSCS, CMS, and IPCS.

VIRTUAL MACHINE/PERFORMANCE ENHANCEMENT (VM/PE): This software product enables an Amdahl user to run the IBM MVS or SVS control program on the same computer as the IBM VM/370 control program. Amdahl claims that the utilization of VM/PE offers significant and immediate performance improvements to the user. These improvements, according to Amdahl, could mean that users will experience MVS production operating system (P/OS) throughput with VM/370 that could be 94 to 97 percent of the MVS native-state throughput. The percentages are based on a 12-megabyte 470V/7 with dedicated MVS channels and no other virtual machine activity.

VM/PE implements a new dispatching interface, P/OS handling of its dedicated channel I/O operations, a restart facility for VM/370 after a control program termination without disturbing the P/OS virtual machine executive within VM/PE, and more accurate P/OS CPU time accounting. VM/PE provides increased P/OS performance by eliminating the management of shadow page tables, most privileged instruction simulation, and VM/370 control program handling of P/OS virtual machine I/O operations. VM/PE masks I/O interrupts for P/OS dedicated channels while VM/370 is in control. VM/PE Release 2.0 adds support of dedicated channel I/O masking to reduce control changes between the P/OS and VM/370. Release 2.0 also provides improved logic to reduce page zero swap overhead and a new function for the VM/370. Release 2.1 provides a Performance Monitor that collects various data from VM/370, and makes it available for fine-tuning the system's overall performance.

VM/PE provides support for the following program product releases:

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Product	Release 2.5	Release 3.0
VM/370	6	*
VM/BSE	2.0	*
VM/SE	2.0	*
VM/SP	*	1.0
SVS	1.7	1.7
MVS	3.7 or 3.8	3.8
MVS/SE	1.0 or 2.0	2.0
MVS/SEA	1.1 or 2.1	2.1
MVS/SP	*	1.0

*Not supported by this release

VM/SOFTWARE ASSIST (VM/SA): This AIDS (Amdahl Internally Developed Software) program product can enhance performance under VM/370 by improving VM/370 instruction simulation. It provides the functional equivalent of IBM's Virtual Machine Assist without the need for additional hardware. VM/SA can co-exist with VM/PE. Combining the two products creates an even more efficient operating environment for VM/370.

MVS/SE ASSIST: This software package is designed to emulate the microcoded MVS enhancements (System/370 Extended Facility) IBM provided in its 303X processors. MVS/SE Assist operates on all 470 processors without modifications to CPU hardware or the MVS/SE code and requires about 1500 bytes of main memory. It can also be installed on IBM 370/158 and 370/168 uniprocessors that do not have the Extended Facility feature. Benchmarks performed by Amdahl indicate a 13 percent drop in supervisor state execution and a 12 percent improvement in throughput with MVS trace on.

MVS/SE Assist is activated upon execution of a System/370 extended instruction by the 470. This is done by installing an MVS/SE Assist routine to precede the program check first-level interrupt handler. This routine intercepts the operation exception program check so that the program check PSW can be analyzed to determine the type of operation requested. MVS/SE Assist normally replaces the interrupted instruction with a branch to an appropriate routine for simulation of the proper microcode.

MVS/SE SUPPORT: This product is functionally equivalent to MVS/SE Assist, and is designed to run on multiprocessor and attached-processor configurations of the 370/158 and 370/168 that do not have Extended Facilities installed.

VM/EXTENDED CHANNEL SUPPORT (VM/ECS): Used in conjunction with Amdahl's 470/Extended Channels hardware; this program product provides support for up to 32 channels operating in a VM environment. The software also supports Amdahl's MVS/ECS program product.

MVS/EXTENDED CHANNEL SUPPORT (MVS/ECS): Similar to VM/ECS, MVS/ECS can support up to 32 channels in a 470 system. MVS/ECS does not, however, extend the maximum number of controllers, devices, or optional channel paths that can be configured under MVS.

UNIVERSAL TIMESHARING SYSTEM (UTS): A powerful, user-oriented, time-sharing system, UTS is based on the UNIX operating system (Version 7.0) developed by Bell Laboratories. UTS operates as a virtual machine under VM/370 or VM/SP. It features asynchronous processing, simplified I/O interfaces, a powerful text processor, full-screen processing capabilities, flexible hierarchical file structures, RJE functions, and system status reporting. UTS is currently available.

AMDAHL INTERNALLY DEVELOPED SOFTWARE (AIDS) is a class of software designed to improve system performance and productivity of the DP staff. Software is developed for the AIDS program by Amdahl employees as software solutions to particular customer problems accrue. All AIDS programs must meet the established criteria of improving performance and/or productivity, and must meet Amdahl standards for maintenance, ease of installation, and quality of documentation and coding. The program's author or representative remains responsible for product support for one year after announced program availability. AIDS products are provided "as is" without warranty either expressed or implied.

IMS/VS HDAM OPTIMIZER: The IMS/VS HDAM Optimizer is the first AIDS software released by Amdahl. It was designed to improve performance when using IMS/VS HDAM data bases. The IMS/VS HDAM Optimizer determines the optimal placement of data during normal data base reorganization, thus reducing the number of physical I/O operations necessary to process a HDAM data base. Amdahl estimates that the number of I/O requests is reduced by 10 to 15 percent. The Optimizer supports all presently existing IMS/VS options and requires no source code modifications to any presently existing IMS/VS routines, user routines, or control blocks.

ACP/SYSTEM ERROR DUMP ANALYSIS: This program product is an AIDS facility used to analyze memory dumps on-line in conjunction with the Airlines Control Program (ACP). It is designed to facilitate rapid problem solving when using the large amounts of data associated with ACP. ACP/SEDA operates in an MVS environment with VSAM. It can be used in a conversational mode under TSO. It can also operate in an MVS environment with a VM/370 Release 5 or 6 system.

PRICING

The Amdahl 470 systems are offered for purchase or for lease under two- or four-year operating lease plans. Leases may be renewed for 12-month periods. Lease payments must be made monthly in advance. Lease payments include the lessee charge, property taxes, and insurance, but not maintenance charges. The minimum lease term for a system upgrade is 12 months. Leases can be terminated after two years upon payment of 30 percent of the total remaining rental payments. A 90-day written notice is required for cancellation. For users wishing to purchase leased equipment, purchase credits of 50 percent of each monthly payment are allowed to a maximum aggregate credit of 50 percent of the purchase price. The purchase credit applies either to the original lessee or the current lessee.

Monthly maintenance charges are not included in lease charges. Maintenance is provided for 24 hours per day and 7 days per week.

Amdahl maintains a Software Systems Support (SSS) group in Sunnyvale, California that supplies its own versions of the supported IBM system releases to Amdahl users. The SSS group also issues Amdahl corrections to the IBM Program Temporary Fix (PTF) tapes.

The Field Support center (FSC), also located in Sunnyvale, California, helps insure a smooth transition at installation time. The FSC also is chartered to analyze and correct problems in supported operating systems.

Amdahl 470

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.*	2-Year Lease	4-Year Lease
PROCESSORS AND MAIN MEMORY					
470V/7C	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below:				
	With 4,194,304 bytes of main memory and:				
	8 channels	$1,050,000	$7,650	$55,025	$42,500
	With 8,388,608 bytes of main memory and:				
	8 channels	1,200,000	9,550	67,425	52,150
	With 12,582,912 bytes of main memory and:				
	8 channels	1,350,000	11,450	79,825	61,800
	With 16,777,216 bytes of main memory and:				
	8 channels	1,500,000	13,350	92,225	71,450
470V/7B	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below:				
	With 4,194,304 bytes of main memory and:				
	8 channels	1,250,000	9,240	57,475	44,635
	12 channels	1,400,000	9,740	64,600	50,285
	16 channels	1,550,000	10,240	71,725	55,935
	With 8,388,608 bytes of main memory and:				
	8 channels	1,400,000	11,140	68,875	54,285
	12 channels	1,550,000	11,640	77,000	59,935
	16 channels	1,700,000	12,140	84,125	65,585
	With 12,582,912 bytes of main memory and:				
	8 channels	1,550,000	13,040	82,175	63,935
	12 channels	1,700,000	13,540	89,300	69,585
	16 channels	1,850,000	14,040	96,425	75,235
	With 16,777,216 bytes of main memory and:				
	8 channels	1,700,000	14,940	94,475	73,585
	12 channels	1,850,000	15,440	101,600	79,235
	16 channels	2,000,000	15,940	108,725	84,885
470V/7A	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below:				
	With 4,194,304 bytes of main memory and:				
	8 channels	1,475,000	9,540	64,940	50,595
	12 channels	1,625,000	10,040	72,065	56,245
	16 channels	1,775,000	10,540	79,190	61,895
	With 8,388,608 bytes of main memory and:				
	8 channels	1,625,000	11,440	77,340	60,245
	12 channels	1,775,000	11,940	84,465	65,895
	16 channels	1,925,000	12,440	91,590	71,545
	With 12,582,912 bytes of main memory and:				
	8 channels	1,775,000	13,340	89,740	69,895
	12 channels	1,925,000	13,840	96,865	75,545
	16 channels	2,075,000	14,340	103,990	81,195
	With 16,777,216 bytes of main memory and:				
	8 channels	1,925,000	15,240	102,140	78,545
	12 channels	2,075,000	15,740	109,265	85,195
	16 channels	2,225,000	16,240	116,390	90,845
470V/7	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below:				
	With 4,194,304 bytes of main memory and:				
	12 channels	1,975,000	10,270	78,405	61,310
	16 channels	2,125,000	10,770	85,530	66,960
	With 8,388,608 bytes of main memory and:				
	12 channels	2,125,000	12,170	90,805	70,960
	16 channels	2,275,000	12,670	97,930	76,610

*Includes 24-hour 7-day service; applies to both purchased and leased systems.

Amdahl 470

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.*	2-Year Lease	4-Year Lease
PROCESSORS AND MAIN MEMORY (Continued)					
470V/7	With 12,582,912 bytes of main memory and:				
	12 channels	2,275,000	14,070	103,205	80,610
	16 channels	2,425,000	14,570	110,330	86,260
	With 16,777,216 bytes of main memory and:				
	12 channels	2,425,000	15,970	115,605	90,260
	16 channels	2,575,000	16,470	122,730	95,910
470V/8	CPU Complex; includes 64K-byte buffer storage console with maintenance processor, and power distribution unit; main memory and channels as indicated below:				
	With 4,194,304 bytes of main memory and:				
	12 channels	2,175,000	10,750	81,935	66,450
	16 channels	2,325,000	11,250	92,060	72,100
	With 8,388,608 bytes of main memory and:				
	12 channels	2,325,000	12,650	97,335	76,100
	16 channels	2,475,000	13,150	104,460	81,750
	With 12,582,912 bytes of main memory and:				
	12 channels	2,475,000	14,550	109,735	85,750
	16 channels	2,625,000	15,050	116,860	91,400
	With 16,777,216 bytes of main memory and:				
	12 channels	2,625,000	16,450	122,135	95,400
	16 channels	2,775,000	16,950	129,260	101,050
MEMORY AND PROCESSOR OPTIONS					
	4-Megabyte Memory Increment for 470V/7 Series and 470V/8	150,000	2,260	15,500	12,065
	Extended Memory, availability to be announced 1st quarter 1982	150,000	—	6,250	5,000
	Additional 470 Series Channels; requires minimum 16 channels with CPU complex:				
	24 channels	425,000	2,260	20,615	16,040
	28 channels	575,000	2,760	27,740	21,690
	32 channels	725,000	3,260	34,865	27,340
	Four-Channel Group	175,000	500	8,400	6,775
	Eight-Channel Group, above 16 channels	475,000	2,260	25,775	22,050
	4,096 Subchannels (per Channel Unit)	50,000	—	3,125	2,500
	High-Speed Channel Feature (provides two Data Streaming channels per four-channel group)	40,000	30	1,420	1,135
	Channel to Channel Adapter	32,500	—	1,000	900
	Two-Byte Interface	1,400	—	50	40
	Hardware Monitor Interface for 470V/7C through 470V/8	40,000	150	1,865	1,400
	Field Upgrade 470V/7C to 470V/7B	250,000	1,590	3,550	2,900
	470V/7B to 470V/7A	275,000	300	6,400	5,125
	470V/7A to 470V/7	400,000	230	7,800	6,500
	470V/7 to 470V/8	250,000	480	7,200	5,775

*Includes 24-hour/7-day service; applies to both purchased and leased systems.

SOFTWARE PRICES

	Field Installation Charge	Factory Installation Charge	Comments
470/Accelerator Hardware for 470V/7C, 470V/7B, 470V/7A	$1,500	$1,000	No charge for first month plus $90 for each additional metered hour thereafter
470/Extended Performance Accelerator Hardware for 470V/7B only	3,000	2,500	No charge for first month plus $300 for each additional metered hour thereafter

Amdahl 470

SOFTWARE PRICES

LEASE OR LICENSE ONLY PRODUCTS

	Monthly License	
VM/Performance Enhancement		
Release 3.0	$1,750	per processor
MVS/SE Support	1,750	per complex at Amdahl sites
MVS/SE Assist	250	per processor
VM/Extended Channel Support	1,000	per processor
MVS/Extended Channel Support	500	per processor
Universal Timesharing System (UTS)	3,000	
Amdahl Internally Developed Software (AIDS)		
IMS/VS HDAM Optimizer	225*	per processor
ACP/System Error Dump Analysis	500	per processor; for initially designated processor only; no charge for additional processors on site
VM/Software Assist	500	—

*24-month period only.